

WHAT IS CLAIMED IS:

1. A method of fabricating a memory device including a plurality of magnetoresistive memory cells, the method comprising the steps of:

forming a first ferromagnetic layer;

flattening an exposed surface of the first layer; and

5 forming a second ferromagnetic layer atop the first ferromagnetic layer, the first and second ferromagnetic layers being ferromagnetically coupled; whereby flattening the exposed surface reduces the ferromagnetic coupling between the first and second ferromagnetic layers.

2. The method of claim 1, further comprising the steps of pinning one of the first and second layers; and forming an insulating tunnel barrier atop the first layer, the barrier being formed prior to forming the second layer, the second layer also being formed atop the barrier.

3. The method of claim 1, wherein the flatness of the first ferromagnetic layer is tuned to adjust electrical response.

4. The method of claim 1, wherein the exposed surface is flattened to a critical flatness.

5. The method of claim 1, wherein the exposed surface is flattened by ion etching.

6. The method of claim 1, wherein edge grain angles at the exposed surface are also reduced.

7. A method of fabricating an MRAM device, the method comprising the steps of:

depositing a first ferromagnetic layer; and

flattening an exposed surface of the first layer, the exposed surface
5 being flattened prior to depositing other layers atop the first ferromagnetic
layer.

8. The method of claim 7, wherein the exposed surface is
flattened to a critical flatness.

9. The method of claim 7, wherein the exposed surface is
flattened by ion etching.

10. The method of claim 7, wherein edge grain angle at the
exposed surface is also reduced.

11. The method of claim 7, further comprising the steps of
forming an insulating tunnel barrier atop the first layer and a second
ferromagnetic layer atop the barrier, the first and second layers being AF
coupled; wherein the exposed surface of the bottom FM layer is flattened to
5 tune the AF coupling to a desired level.

12. An SDT junction of a memory cell for an MRAM device, the
junction comprising:

a bottom ferromagnetic layer, the bottom ferromagnetic layer having
flattened peaks;

5 an insulating tunnel barrier atop the bottom ferromagnetic layer; and
a top ferromagnetic layer atop the insulating tunnel barrier.

13. The junction of claim 12, wherein angle from the top of a
grain to an intersection with an adjacent grain is between about three and six
degrees.

14. The junction of claim 12, wherein the flattened peaks have a valley-to-peak height difference of no more than about one nanometer.

15. The junction of claim 12, wherein the junction has a resistance of less than about $10 \text{ K}\Omega\cdot\mu\text{m}^2$.

16. The junction of claim 12, wherein the top and bottom layers are AF coupled; wherein the peaks are flattened to tune the AF coupling to a desired level.

17. An MRAM device comprising:

an array of memory cells, each memory cell including an SDT junction, each SDT junction including a bottom ferromagnetic layer, each bottom ferromagnetic layer having an upper surface, each upper surface having a

5 valley-to-peak height variation of no more than about one nanometer; a plurality of word lines extending memory cell rows of the array; and a plurality of bit lines extending along memory cell columns of the array.

18. The device of claim 17, wherein resistance variation of the junctions across the entire array is no more than about 4%.

19. The device of claim 17, wherein angle from the top of a grain to an intersection with an adjacent grain is between and three and six degrees.

20. The device of claim 17, wherein the junctions have a resistance of less than about $10 \text{ K}\Omega\cdot\mu\text{m}^2$.